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# System-in-Package



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**14<sup>th</sup> June 2007: Hosted by TWI, Great Abington, Cambridge**

*A joint NMI, TWI seminar covering technical and commercial aspects of this rapidly growing, high density, high performance and low cost-per-function packaging technology for microelectronics systems integration*

Presentations include:

Keynote: New developments and applications for SiP,  
*Tim Lenihan and Jan Vardaman, TechSearch International*

Industrial perspectives in System-in-Package, *Brad Factor, ASE*

System-in-Package design methodologies, *Gary Hinde, Cadence*

System-in-Package manufacturing solutions, *Bernie Ramsay, UNISEM*

System-in-Package with silicon integrated passives, *Alain Rougier, NXP*

SiP solutions in the medical arena, *Piers Tremlett, Zarlink Semiconductor*

SiP technologies and wireless communications, *Andrew Holland, CSR*

Advanced design, partitioning and test for SiP, *David Pedder, TWI*

System-in-Package substrate options, *Bob Hunt, CMAC*

*Who should attend?*

*System designers, device designers, packaging and interconnection engineers, technology developers, manufacturing, device and systems applications engineers in the electronics, photonics and sensors industries*

The fee for this seminar is £75.00 + VAT

For registration please return a complete form to [rachel.wall@twi.co.uk](mailto:rachel.wall@twi.co.uk)

or visit [www.eventsforce.net/07SIP](http://www.eventsforce.net/07SIP) to register online

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## Programme Detail

*The National Microelectronics Institute (NMI) and TWI are organising a joint one-day seminar on System-in-Package trends, technologies and applications which will be held at TWI, Granta Park, Cambridge on 14th June 2007. This joint NMI/TWI seminar provides a very timely technical and commercial overview of all aspects of this rapidly growing, high density, high performance and low cost-per-function packaging technology for microelectronics systems integration. The seminar is kindly sponsored by Unisem Europe and by Cadence and is also supported by the Photonics KTN, the EPPIC Faraday Partnership and by IMAPS UK.*

The new System-in-Package (SiP) paradigm in electronics product implementation allows the mixing of optimum active and passive device technologies in bare die format within a single package outline for cost effective, high performance, short time-to-market functionality well matched to a wide range of low, medium and high volume electronics product applications. The novel addition of embedded passive component technology within such SiP modules also promises further performance, size, weight and cost benefits. The technology has driven the development of robust design routes for right-first-time design and is now seeing volume applications for a range of communications and portable system products where cost-per-function, size, weight and performance are all critical factors.

This System-in-Package seminar provides a unique opportunity for system designers, device designers, packaging and interconnection engineers, technology developers, manufacturing, device and systems applications engineers in the electronics, photonics and sensors industries to gain an overview of UK, European and International developments, technology capabilities and trends and to network with colleagues, design and technology providers in this key technology area.

### **The provisional seminar programme is as follows:**

- 09:15 *Coffee and Registration*
- 09:45 *Welcome and Introduction*  
Paul Jarvie, NMI  
David Pedder, TWI
- 10:00 *Keynote - New developments and applications for SiP, Tim Lenihan and Jan Vardaman - TechSearch International, Austin, USA*
- 10:45 *Refreshment break*
- 11:00 *System-in-Package with silicon integrated passives, Alain Rougier, NXP*
- 11:30 *System-in-Package design methodologies, Gary Hinde, Cadence*
- 12:00 *System-in-Package Manufacturing Solutions, Bernie Ramsay, UNISEM*
- 12:30 *Lunch and networking*
- 13:15 *Industrial perspectives in System-in-Package, Brad Factor, ASE*
- 13:45 *SiP Solutions in the Medical Arena, Piers Tremlett, Zarlink Semiconductor*
- 14:15 *SiP Technologies and Wireless Communications, Andrew Holland, CSR*
- 14:45 *Refreshment break*
- 15:00 *Advanced Design, Partitioning and Test for SiP, David Pedder, TWI*
- 15:30 *System-in-Package Substrate Options, Bob Hunt, CMAC*
- 16:00 *Close*

